BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

By this Amendment, Applicants amend claims 27, 28, and 31-33 to more appropriately define the present invention. Claims 27, 28, and 30-33 remain pending.

In the Office Action ("OA"), the Examiner objected to the drawings; maintained the rejection of claims 27, 28, and 30-33 under 35 U.S.C. § 112, second paragraph; and maintained the rejection of claims 27, 28, and 30-33 under 35 U.S.C. § 103(a) as unpatentable over Kume et al., U.S. Patent No. 5,188,976 ("Kume") in view of Tada, U.S. Patent No. 5,497,021 ("Tada").

I. Response to Drawing Objections

The Examiner alleged that the drawings filed on October 17, 2000[1] are objected to by the draftsperson for the reasons stated in an enclosed form PTO-948. (OA at 2.) However, a form PTO-948 was not enclosed with the current Office Action and the Office Action Summary, form PTO-326, did not indicate that a form PTO-948 was attached. Furthermore, the Examiner indicated, in the Office Action mailed June 6, 2002, that the drawings were accepted. Accordingly, Applicants request clarification on the status of the drawings.

II. Response to Rejection of Claims 27, 28, and 30-33 under 35 U.S.C. § 112, second paragraph

The Examiner rejected claims 27, 28, and 30-33 under section 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter Applicants regard as the invention. Particularly, the Examiner alleged that the phrase "a side wall of said first gate electrode at one end of a channel direction is connected to a side wall of said second gate electrode at one end of the channel direction" renders the claim indefinite

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

[1] The Examiner indicated that the drawings were filed on October 1, 2000, but the formal drawings were filed on October 17, 2000, together with the subject application.

because the term "the channel" is indefinite since "the channel" has several meanings. (OA at 3.)

Applicants amend claim 27 to remove reference to the channel region and describe the gate electrode connection with reference to the isolation element. Specifically, claim 27 now recites, *inter alia*, "wherein a side wall of the first gate electrode is connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction." Applicants submit that claim 27 is clear and definite. Accordingly, Applicants request that the Examiner withdraw the rejection of claim 27 under section 112, second paragraph.

Further, the Examiner alleged that claims 28 and 30-33 are rejected for depending upon rejected claim 27. (OA at 3.) As mentioned above, Applicants submit that claim 27 is clear and definite. Accordingly, Applicants request that the Examiner withdraw the rejection of claims 28 and 30-33 under section 112, second paragraph.

In addition, the Examiner alleged that the phrase "and said side wall of said first gate electrode is connected to the side wall of said second gate electrode and a side wall of said side insulator film," as recited in claim 33 is unclear. (OA at 3.) Applicants amend claim 33 to more appropriately define the side wall connections. Specifically, claim 33 now recites "wherein said second transistor further comprises a polysilicon layer formed on the second insulation film formed on the substrate, and a side insulator film formed on a side wall of the second insulation film and a side wall of the polysilicon layer, said second gate electrode is formed on the polysilicon layer, the side wall of said first gate electrode is directly connected to a side wall of said second gate electrode and connected to the side wall of the second insulation film and the side wall of the polysilicon layer via the side insulator film. Applicants submit that claim 33 is

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

clear and definite. Accordingly, Applicants request that the Examiner withdraw the rejection of claim 33 under section 112, second paragraph.

III. Rejection of claims 27, 28, and 30-33 under 35 U.S.C. § 103(a)

The Examiner rejected claims 27, 28, and 30-33 under section 103(a) as unpatentable over Kume in view of Tada. In response, Applicants submit that a *prima facie* case of obviousness has not been established for claims 27, 28, and 30-33 because Kume and Tada, when taken alone or in combination, fail to teach or suggest all the claim elements.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Furthermore, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03, ed. 8, rev. 1 (Feb. 2003) (quoting *In re Wilson*, 424 F.2d 1382, 1385 (C.C.P.A. 1970)). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. M.P.E.P. § 2143 at 2100-122 to 127.

Claim 27 is directed to a semiconductor device comprising a combination of elements including, *inter alia*, "a first transistor formed on [a] first region of the substrate and including a first insulation film and a first gate electrode arranged along a first direction; and a second transistor formed on [a] second region of the substrate and including a second insulation film and a second gate electrode arranged along the first direction, wherein a side wall of the first gate electrode is connected to a side wall of the second gate electrode above [an] isolation element when viewed from a direction perpendicular to the first direction." (emphasis added.)

In rejecting claim 27, the Examiner admitted that Kume does not disclose that first and second gate electrodes are connected at a side wall. (OA at 4.) Nonetheless, the Examiner

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

alleged that Tada discloses a direct connection between gate electrodes at the side walls. (OA at 4.) Specifically, the Examiner alleged that Tada discloses a direct connection between gate electrodes 13a and 13b by elements 21a and 21b. (OA at 4, 8).

Tada, Fig. 1, illustrates "a schematic cross sectional view showing a structure of a semiconductor device." Tada, col. 4, lines 44-46. However, Tada, Fig. 1, fails to illustrate that the sidewalls of gate electrodes 13a and 13b are connected. *See* Tada, Fig. 1. Nonetheless, the Examiner relied on Fig. 3d for support for his allegations. Specifically, the Examiner alleged that "the structure in fig. 3 is the final structure obtained by steps in figs. 3a-3d" and "is a different embodiment from that described in fig. 1." (OA at 9.) Applicants submit that the Examiner has misinterpreted Tada.

Applicants direct the Examiner to Tada's disclosure at col. 4, ll. 50-52 which states "FIGS. 3(a) to 3(d) are step cross sectional views showing a part of the remaining steps of the production process of the semiconductor device shown in FIG. 1." Tada, col. 4, ll. 50-52. The Examiner ignores the fact that Fig. 3d does not even illustrate gate electrodes 13a and 13b, but only illustrates polysilicon layer 23 prior to the formation of gate electrodes 13a and 13b. Tada, col. 7, lines 10-14. Gate electrodes 13a and 13b are formed in an unillustrated step between the process step illustrated in Fig. 3d and the final product illustrated in Fig. 1. Specifically, Tada recites

> Then, on the surface side of the second polycrystalline silicon layer 23 is formed a resist mask layer. Then after patterning, dry etching and removing the resist layer, polycrystalline silicon layers 23a and 23b (gate electrodes 13a and 13b) are left only in a desired region of the low voltage drive circuit portion 1a. Tada, col. 7, ll. 10-14 (emphasis added).

In other words, silicon layer 23 in formed (illustrated in Fig. 3d) and patterned into gate electrodes 13a and 13b which are located in region 1a (illustrated in Fig. 1). Thus, gate

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

electrodes 13a and 13b do not have any direct connection with elements 23a and 23b because they are formed in separate regions 1a and 1b. Thus, the Examiner has incorrectly asserted that side walls of gate electrodes 13a and 13b are connected by polysilicon layer 21a and 21b.

Additionally, the Examiner cited col. 8, line 1, of Tada to support his argument that Fig. 3d illustrates gate electrodes 13a and 13b. (OA at 9.) However, this citation actually supports Applicants' position since the cited text is describing the semiconductor device illustrated in Fig. 1. *See* Tada, col. 7 line 36 to col. 8, line 2 (describing process formed on the device illustrated in Fig. 1).

The only disclosure in Tada regarding the connection of gate electrodes 13a and 13b can be found at col. 8, ll. 5-7. Specifically, Tada recites "[f]or example, the gate electrode 13a can be electrically connected to the gate electrode 13b directly without through aluminum electrode." Tada, col. 8, ll. 5-7. Regardless, Tada merely recites the possibility that the gate electrodes can be connected, and Tada does not disclose that the gate electrodes are, in fact, connected at the side walls.

Therefore, Tada fails to teach or suggest at least "wherein a side wall of the first gate electrode is connected to a side wall of the second gate electrode above [an] isolation element when viewed from a direction perpendicular to the first direction," as recited in claim 27. Since Tada fails to cure the deficiencies of Kume, Kume and Tada, taken alone or in combination, fail to teach or suggest all the claim elements. Accordingly, a *prima facie* case of obviousness has not been established for claim 27. For at least this reason, claim 27 is allowable.

Claims 28 and 30-33 are allowable at least due to their dependence from allowable claim 27. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

therefrom is nonobvious." M.P.E.P. § 2143.03 at 2100-126 (citing *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988)).

IV. Conclusion

In view of the foregoing, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: November 18, 2003

By: _____
Bryan S. Latham
Reg. No. 49,085

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com